DS255: System Virtualization

Assignment-IV

Total Marks: 36

1. Why all the sensitive instructions need to be a part of privileged instructions to enable ISA virtualizability? Marks - 4

2. Why is it important for the VMM to handle the timer interrupt? What might not be feasible if the timer interrupt control is given to the GuestOS of a VM? Marks – 4 (2+2)

3. What can be the benefit and consequence of running multiple OSes with same privilege on the same hardware? Assume that there is no hypervisor. What other support from hardware is needed to ensure that these multiple OSes operate correctly in such a situation? Assume that each OS is given exclusive access to the resources it requires during execution. Marks – 6 (2+2+2)

4. Under shadow page table method for virtualizing memory, what address mapping is stored in the TLB? Given that the Page table is a 4-level tree, how many tree and page traversals will one translation entail? Marks – 4 (2+2)

5. Latest Intel processor supports 4KB, 2MB and 1GB page sizes. Using the 48-bit virtual address draw the 2D page walk diagram for 2MB and 1GB page size assuming that the page offsets are in LSB position and state how many memory accesses are required to get the address of the page frame. How do large page sizes help in reducing page fault latencies? Marks-10 (4+4+2)

6. Virtual switch in the hypervisor enables NIC virtualization. Explain with a schematic diagram how the network packet reception and transmission workflow is enacted through the I/O virtualization stack. Marks-5

7. List three goals of I/O virtualization. Marks – 3

Last date for submission – March 20, 2020 (Midnight)
Mail the answers in pdf format to – architaghosh@iisc.ac.in